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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/360,472	07/23/1999	RETO STAMM	X-528-US	4229

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XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	17

DATE MAILED: 03/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/360,472	Applicant(s) STAMM ET AL.	
	Examiner Thai Phan	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *19 December 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7 and 15-20* is/are rejected.

7)☒ Claim(s) *8-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☒ Interview Summary (PTO-413) Paper No(s). *17* .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

This Office Action is in response to applicants' amendment filed on Dec. 19, 2003. Claims 1-20 are pending.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-7 and 15-20 are rejected under 35 U.S.C. 103(a) as being obvious over Goslin, US patent no. 6,120,549, in view of Kim US patent no. 6,553,531 B1.

3. The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29,

1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

3.1 As per claim 1, Goslin discloses a method and apparatus for designing and verifying an integrated circuit with feature limitations substantially similar to the claimed invention. According to Goslin, the hardware design and verification method includes steps:

parameterizing circuit functional blocks or logic circuit cores to meet user' specific requirement (col. 3, line 17 to col. 5, line 40),

generating a netlist or RTL model from the set of randomly generated parameter values and device under test for verification (col. 13, lines 30-49, for example),

and verifying or simulating circuit behavior with the RTL model or net list as claimed. Goslin does not especially disclose randomly generating a set of values for parameters of the logic core. Such claimed feature is however well known in the art. In fact, Kim teaches method and system for simulating integrated circuit design. Kim teaches parameter values of the design logic circuits are randomly generated for testing and verification such that the design testing and verification (col. 2, lines 52-57, col. 3, lines 37-50, col. 5, lines 42-53, for example) would be faster and accurate.

This would motivate practitioner in the art at the time of the invention was made to combine Kim teaching of random value generation of design variables in the circuit

design test and verification such as in Goslin parameterized logic cores in order to carry out a faster and accurate test and verification of the design as taught in Kim.

3.2 As per claim 2, Goslin discloses upper and lower limits associated with random parameter values (col. 6, lines 48-62, for example), and generating a new random parameter set for the design to meet design specification (col. 7, line 52 to col. 8, line 10).

3.3 As per claim 3, Goslin discloses weight file or probability function for parameter values generation in order to randomly generating parameter values (col. 9, line 20 to col. 10, line 14).

3.4 As per claim 4, Goslin discloses generating parameter values as input to a graphical user interface (col. 4, lines 26-43, col. 6, line 48 to col. 7, line 25), and replacement values for invalid parameter values to meet design requirement (col. 8, lines 15-60).

3.5 As per claim 5, Goslin discloses a graphical user interface with feature limitations as claimed to allow user interactive with the design process (cols. 6-8).

3.6 As per claims 6 and 7, Goslin discloses generating replacement parameter values for the invalid parameters (col. 8, lines 15-60), and repeating such step for all parameters to meet design requirement.

3.9 As per claim 15, Goslin teaches graphic user interface and interactive means to allow user to key in design parameters selection, change, or set as claimed (col. 4, lines 26-43, col. 6, line 48 to col. 7, line 25).

3.10 As per claim 16, Goslin teaches design order in order to generating parameters for the design, and generating parameter values for the orderly hierarchy of the design process (col. 5, lines 23-65, col. 6, lines 1-18, for example).

3.11 As per claim 17, Goslin teaches design verification including performance a number of design simulation, accumulating of fail test data, recording parameters of the design simulation, etc. in order to verify the design performance.

3.12 As per claim 18, Goslin discloses a method and apparatus for design and verification of integrated circuit with feature limitations substantially similar to the claimed invention. According to Goslin, the hardware design and verification includes steps:

parameterizing circuit functional blocks or logic circuit cores to meet user' specific requirement (col. 3, line 17 to col. 5, line 40),

generating a netlist or RTL model from the set of randomly generated parameter values and device under test for verification (col. 13, lines 30-49, for example),

and verifying or simulating circuit behavior with the RTL model or net list as claimed. Goslin does not expressly disclose randomly generating a set of values for the logic core. Such claimed feature is however well known in the art. In fact, Kim teaches method and system for simulating integrated circuit design. Kim teaches a method of randomly generating parameter values for design logic core to faster and accurate verification of the design circuit (col. 2, lines 52-57, col. 3, lines 37-50, col. 5, lines 42-53, for example).

This would motivate practitioner in the art at the time of the invention was made to combine Kim teaching of random value generation of design variables such as Goslin parameterized logic cores in order to faster and accurately test and verify the design as taught in Kim above.

3.13 As per claim 19, Goslin discloses a method and apparatus for design and verification of integrated circuit with feature limitations substantially similar to the claimed invention. According to Goslin, the hardware design and verification includes steps:

parameterizing circuit functional blocks or logic circuit cores to meet user' specific requirement (col. 3, line 17 to col. 5, line 40),

generating a netlist or RTL model from the set of randomly generated parameter values and device under test for verification (col. 13, lines 30-49, for example),

and verifying or simulating circuit behavior with the RTL model or net list as claimed. Goslin does not expressly disclose randomly generating a set of values for the logic core. Such claimed feature is however well known in the art. In fact, Kim teaches method and system for simulating integrated circuit design. The method requires according to Kim teaches randomly generating parameter values for design logic core such that the design testing and verification will be faster and accurate (col. 2, lines 52-57, col. 3, lines 37-50, col. 5, lines 42-53, for example).

This would motivate practitioner in the art at the time of the invention was made to combine Kim teaching of random value generation of design variables such as Goslin

parameterized logic cores in order to faster and accurately test and verify the design as taught in Kim above.

3.14 As per claim 20, Goslin discloses a method and apparatus for design and verification of integrated circuit with feature limitations substantially similar to the claimed invention. According to Goslin, the hardware design and verification includes steps:

parameterizing circuit functional blocks or logic circuit cores to meet user' specific requirement (col. 3, line 17 to col. 5, line 40),

generating a netlist or RTL model from the set of randomly generated parameter values and device under test for verification (col. 13, lines 30-49, for example),

and verifying or simulating circuit behavior with the RTL model or net list as claimed. Goslin does not expressly disclose randomly generating a set of values for the logic core. Such claimed feature is however well known in the art. In fact, Kim teaches method and system for simulating integrated circuit design. Kim teaches a method of randomly generating parameter values for design logic core to faster and accurate verification of the design circuit (col. 2, lines 52-57, col. 3, lines 37-50, col. 5, lines 42-53, for example).

This would motivate practitioner in the art at the time of the invention was made to combine Kim teaching of random value generation of design variables such as Goslin parameterized logic cores in order to carry out a faster and accurate test and verification of the design as taught in Kim above.

Allowable Subject Matter

Claims 8-14 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

As per claims 8-14, the claims require steps of "cloning the set of parameter values", and "mutating the sets of parameter values, whereby a mutated set of parameter values is produced" for simulating the circuit netlist as claimed. The closest prior art in the record does not show or suggest these features.

Response to Arguments

Applicant's arguments filed on Dec. 19, 2003 have been fully considered but they are not persuasive.

In response to applicants' argument Goslin may not be considered to preclude patentability in any rejection under 35 USC 103 (a) art rejection (page 2, last paragraph to page 3), the examiner disagrees with the reasons below:

Applicant has provided evidence in this file showing that the invention was owned by, or subject to an obligation of assignment to, the same entity as in US patent no. 6,120,549, issued to Goslin at the time this invention was made. Accordingly, US patent no. 6,120,549 is disqualified as prior art through 35 U.S.C. 102(f) or (g) in any rejection under 35 U.S.C. 103(a) in this application. However, this applied art additionally qualifies as prior art under another subsection of 35 U.S.C. 102 and accordingly is not disqualified as prior art under 35 U.S.C. 103(a).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art only under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 103(a) might be overcome by: (1) a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not an invention "by another"; (2) a showing of a date of invention for the claimed subject matter of the application which corresponds to subject matter disclosed but not claimed in the reference, prior to the effective U.S. filing date of the reference under 37 CFR 1.131; or (3) an oath or declaration under 37 CFR 1.130 stating that the application and reference are currently owned by the same party and that the inventor named in the application is the prior inventor under 35 U.S.C. 104, together with a terminal disclaimer in accordance with 37 CFR 1.321(c). For applications filed on or after November 29, 1999, this rejection might also be overcome by showing that the subject matter of the reference and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person. See MPEP § 706.02(l)(1) and § 706.02(l)(2).

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to examiner Thai Phan whose telephone number is 703-305-3812.

5. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thai Phan
Mar. 05, 2004

Thaiphan
Thai Phan
Patent Examiner
AU: 2128